CLAIMS

What is claimed is:

1. A data processing system performing a software initialization using an initialization program after performing an initialization in response to a reset signal, the system comprising:

an address selecting section selecting a start address of the initialization program stored in a memory based on an address selection signal; and

an area design register to designate an address area of the memory.

2. The data processing system according to claim 1, wherein the initialization is a hardware initialization.

3. A data processing system performing software initialization using an initialization program after an initialization in response to a reset signal, the system comprising:

an access inhibiting section inhibiting any access request to a memory storing the initialization program based on a start inhibit signal, wherein the initialization program is transferred from an external memory to the memory while the start inhibiting signal is applied.

4. A data processing system comprising data processors connected to a common bus, each of the processors performing software initialization using an initialization program after performing initialization in response to a reset signal, and at least one of the processors comprising:

an address inhibiting section inhibiting any access requests to an external memory storing the initialization program, based on a start inhibiting signal,

wherein the initialization program is transferred from the external memory to a local memory while the access inhibiting section inhibits any access requests to the local memory.

5. A data processing system performing software initialization using an initialization program after performing initialization in response to a reset signal, the system comprising:

a data transferring control section transferring the initialization program from an external memory to a local memory of another processor while the processor is inhibited to access requests to the local memory.

6. A data processing system comprising data processors connected to a common bus, each of the processors performing software initialization using an initialization program after performing initialization in response to a reset signal, and at least one of the processors comprising:

a data transferring control section transferring the initialization program from an external memory to a local memory of one other processor while the other processor is inhibited to access requests to the local memory.

7. A data processing system performing a second initialization using an initialization program after a first initialization, the system comprising:

a reset register storing a reset signal,

wherein the initialization program executes processing selectively based on the reset signal.

8. The data processing system according to claim 7, wherein a memory storing a start address of the initialization program stored is selected based on the reset signal.

9. The data processing system according to claim 8, wherein the memory is a local memory or an external memory.

10. The data processing system according to claim 7, wherein the initial reset signal is one of a plurality of reset signals.

11. A data processing system performing software initialization using an initialization program in response to a reset signal, the system comprising:

an address designation section to designate an address area of a memory that stores a start address of the initialization program based on the reset signal.

12. The data processing system according to claim 11, wherein the initial reset signal is one of a plurality of reset signals.

13. The data processing system according to claim 11, further comprising:

a reset register storing the reset signal.

14. A data processing method performing software initialization using an initialization program in response to a reset signal, the method comprising:

receiving the reset signal; and

executing processing selectively based on the reset signal.

15. The data processing method according to claim 14, wherein a memory storing a start address of the initialization program stored is selected based on the reset signal.

16. The data processing method according to claim 15, wherein the memory is a local memory or an external memory.

17. The data processing method according to claim 14, wherein the initial reset signal is one of a plurality of reset signals.

18. A data processing method performing software initialization using an initialization program in response to a reset signal, the method comprising:

receiving the reset signal; and

designating an address area of a memory that stores a start address of the initialization program based on the reset signal.

19. A data processing method performing software initialization using an initialization program after performing initialization in response to a reset signal, the method comprising:

performing the initialization;

setting the reset signal in a reset register;

checking the reset signal in the reset register; and

performing the software initialization selectively based on the reset signal.

20. The data processing method according to claim 19, wherein the software initialization program starts to execute at a start address stored in one of a local memory and an external memory.

21. The data processing method according to claim 20, wherein the local memory is a high-speed memory and the external memory is a low-speed memory.

22. A data processing method performing software initialization using an initialization program in response to a reset signal, the method comprising:

storing a reset signal to a reset register;

selecting an address of the initialization program in a memory;

reading the reset signal in the reset register;

branching the initialization program to execute the initialization program selectively.

23. The data processing method according to claim 22, wherein the memory is one of a local memory and an external memory.

24. An initialization method initializing a processor in response to a reset signal, the method comprising:

performing a first initialization for the processor;

releasing the processor from the first initialization;

designating an address of a second initialization in a memory based on the reset signal; and

performing the second initialization.

25. The initialization method according to claim 24, further comprising:

setting the reset signal in a reset register; and

checking the reset signal in the reset register for the second initialization.